AMENDMENTS TO THE CLAIMS

Claim 1 (Currently Amended) A method of manufacturing a multi-layer circuit board in which a core circuit board having a circuit pattern thereon and a prepreg sheet having a through-hole filled with conductive paste are laminated, the method comprising:

forming a laminated structure from (i) a laminated member including the core circuit board and the prepreg sheet and (ii) a pair of lamination plates, the laminated member being sandwiched between the pair of lamination plates; and

applying heat and pressure to the laminated structure,

wherein a thermal expansion coefficient of the core circuit board is in a range of 10 x 10^{-6}/°C to 12 x 10^{-6}/°C,

wherein the laminated member further includes a layer of metal foil on both surfaces thereof that are sandwiched between the pair of lamination plates, such that each layer of metal foil is sandwiched between the pair of lamination plates,

wherein, a thermal expansion coefficient of the pair of lamination plates is equivalent to [[a]] the thermal expansion coefficient of the core circuit board, and

wherein the metal foil is made of copper, and the thermal expansion coefficient of the pair of lamination plates is smaller than a thermal expansion coefficient of the metal foil.

Claim 2 (Previously Presented) The method of manufacturing a multi-layer circuit board of Claim 1, wherein the prepreg sheet includes a base and two resin layers being impregnated with

the base, and wherein a total thickness of the two resin layers formed on both surfaces of the base is at least 20 μm.

Claim 3 (Previously Presented) The method of manufacturing a multi-layer circuit board of Claim 1, wherein the core circuit board includes at least four layers.

Claim 4 (Previously Presented) The method of manufacturing a multi-layer circuit board of Claim 1, wherein the core circuit board is not less than one times a thickness of the prepreg sheet.

Claim 5 (Cancelled)

Claim 6 (Previously Presented) The method of manufacturing a multi-layer circuit board of Claim 1, wherein the laminated member is formed from the core circuit board and the prepreg sheet being alternately laminated, so as to have two or more layers.

Claim 7 (Previously Presented) The method of manufacturing a multi-layer circuit board of Claim 1, wherein:

a buffer material is disposed at an outside of the laminated structure;

the laminated structure is placed on a carrying plate;

the laminated structure undergoes heat and pressure through the buffer material and the carrying plate; and

a thermal expansion coefficient of the carrying plate equals the thermal expansion coefficient of the pair of lamination plates.

Claim 8 (Previously Presented) The method of manufacturing a multi-layer circuit board of Claim 1, wherein:

a buffer material is disposed at an outside of the laminated structure;

the laminated structure is placed on a carrying plate;

the laminated structure undergoes heat and pressure through the buffer material and the carrying plate; and

the buffer material is formed of a material capable of accommodating a difference in the thermal expansion of the pair of lamination plates and a thermal expansion of the carrying plate.

Claim 9 (Previously Presented) The method of manufacturing a multi-layer circuit board of Claim 1, wherein the prepreg sheet includes a base impregnated with a resin and wherein a layer of the resin is formed on both surfaces of the base.

Claim 10 (Previously Presented) The method of manufacturing a multi-layer circuit board of Claim 1, wherein the prepreg sheet is a B-staged prepreg in which a woven fabric base is impregnated with a thermosetting resin.

Claim 11 (Currently Amended) The method of manufacturing a multi-layer circuit board of Claim 1, further comprising ~~including~~:

measuring the thermal expansion coefficient of the core circuit board; and

selecting the pair of lamination plates such that the thermal expansion coefficient of the pair of lamination plates is equivalent to the measured thermal expansion coefficient of the core circuit board.

Claim 12 (Currently Amended) The method of manufacturing a multi-layer circuit board of Claim 1, further comprising:

measuring the thermal expansion coefficient of the core circuit board having a predetermined circuit pattern; and

selecting the pair of lamination plates such that the thermal expansion coefficient of the pair of lamination plates is equivalent to the measured thermal expansion coefficient of the core circuit board.

Claim 13 (Previously Presented) The method of manufacturing a multi-layer circuit board of Claim 12, wherein the measuring of the thermal expansion coefficient of the core circuit board includes measuring the thermal expansion coefficient of the core circuit board (i) at two or more positions of the circuit pattern on the core circuit board and (ii) in a range from room temperature to a heat pressing temperature, the measuring being conducted using a thermo-mechanical measurement apparatus.

Claim 14 (Previously Presented) The method of manufacturing a multi-layer circuit board of Claim 12, wherein:

the measuring of the thermal expansion coefficient of the core circuit includes measuring the thermal expansion coefficient of the core circuit board at two or more positions; and

the method further comprises:

calculating an average value of the thermal expansion coefficient of the core circuit board according to the measurement carried out at the two or more positions; and

selecting the pair of lamination plates such that the thermal expansion coefficient of the pair of lamination plates is equivalent to the calculated average value of the thermal expansion coefficient.

Claim 15 (Previously Presented) The method of manufacturing a multi-layer circuit board of Claim 1,

wherein the thermal expansion coefficient of the pair of lamination plates has a permissible range of ± 20% with respect to the thermal expansion coefficient of the core circuit board, and

wherein a thickness of the prepreg sheet is approximately 70 μm.

Claim 16 (Previously Presented) The method of manufacturing a multi-layer circuit board of Claim 15, wherein the thickness of the prepreg sheet after pressing is approximately 60 μm.